

Continuous-Time Bandpass $\Delta\Sigma$ Capacitance-to-Digital Converter

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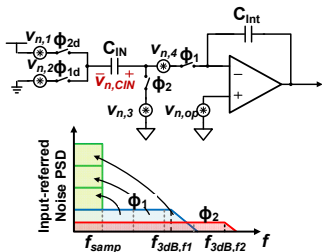
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Abstract

This paper presents an ultra-high-resolution energy-efficient 4th-order continuous-time (CT) bandpass (BP) $\Delta\Sigma$ capacitance-to-digital converter (CDC) where thermal noise folding is avoided by CT operation and power is saved by using a BP $\Delta\Sigma$ architecture. The proposed CDC achieves a resolution of 3.68 aF_{rms} at room temperature while achieving a Schreier figure-of-merit (FoM_S) of 183dB which is more than 2x improvement over the state-of-the-art CDCs.

Introduction

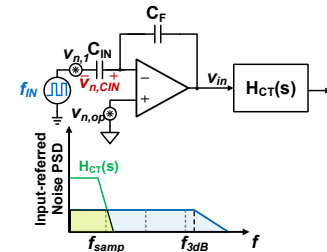
DT- $\Delta\Sigma$ CDC Resolution



$$\frac{C_{n,IN}^2}{V_{DD}^2} \approx \frac{kT \cdot C_{IN}}{V_{DD}^2} \cdot \left(\frac{\frac{7}{3} + R_{ON} \cdot g_m}{1 + R_{ON} \cdot g_m} \right) \geq \frac{2kT \cdot C_{IN}}{V_{DD}^2}$$

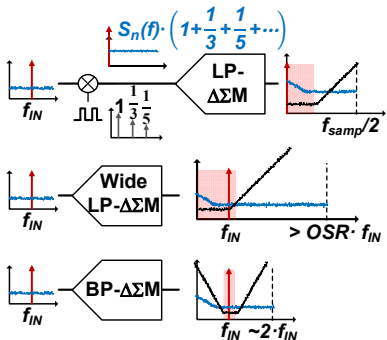
- ✓ DT circuits inevitably increases the in-band noise floor due to noise folding
- ✓ CT circuits significantly reduce the minimum capacitor resolution

CT- $\Delta\Sigma$ CDC Resolution



$$\frac{1}{C_{n,IN}^2} \approx \frac{C_{IN}^2}{V_{DD}^2} \cdot \left(4kTR_{ON} + \frac{16kT}{3g_m} \right) \cdot \frac{\pi}{2} \cdot f_{samp}$$

Energy-Efficient $\Delta\Sigma\text{M}$ Structure

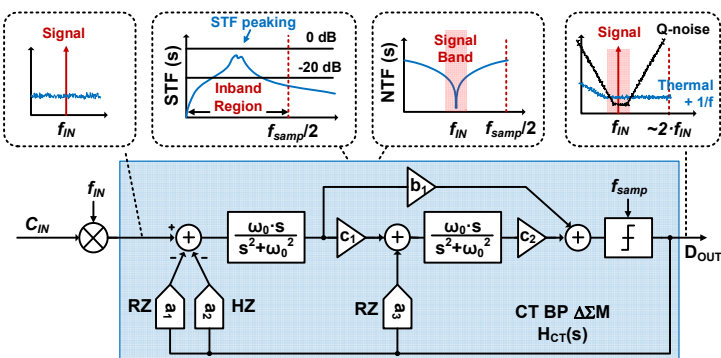


2nd-order noise shaping

Amp. GBW	Loop-filter Power
$(\text{OSR} \cdot f_{\text{IN}}) \cdot 10$	$2 \cdot \left(\frac{10 \cdot \text{OSR}}{10^{2.5}} \right)^2 \cdot P_{\text{BP}}$
$f_{\text{IN}} \cdot 10^{2.5}$	$4 \cdot P_{\text{BP}}$

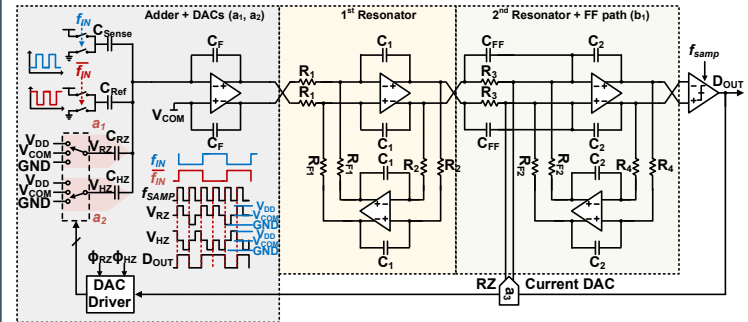
- Gain in the signal band > 50dB
- Gain in $f_{\text{samp}}/2 > 20\text{dB}$.

Proposed Architecture & Implementation



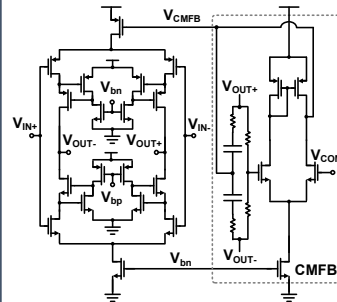
Block Diagram of the Proposed 4th-order CT BP $\Delta\Sigma$ CDC

- ✓ Combination of feedforward and feedback paths



Overall Circuit Schematic of the Proposed CDC

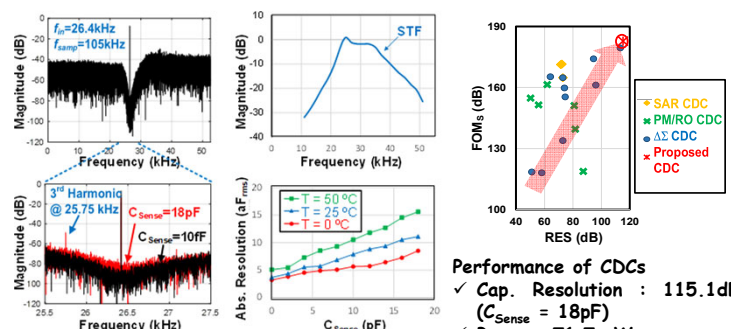
- ✓ Input stage is realized by a capacitive feedback amplifier
- ✓ 2 feedbacks (a_1 , a_2) are realized by charge-domain DACs (C_{HZ}/C_{R2})
- ✓ Active RC resonators are employed as it offers high linearity, parasitic insensitivity, wide input range, and simplicity.



Proposed Inverter-based Amplifier with Gain-boosting

- ✓ Active RC integrator requires a high DC-gain amplifier
- ✓ Achieves high DC gain and low power consumption

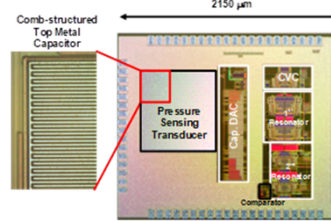
Measurement Results & Conclusion



Performance of CDCs

- ✓ Cap. Resolution : 115.1dB
($C_{\text{Sense}} = 18\text{pF}$)
- ✓ Power : 71.7 μW
- ✓ FoM_W : 0.37 pJ/c.step
- ✓ FoM_c : 183 dB

Measured output spectrum, STF and
cap. Resolution according to C_{Sense}



Die Photograph

	JSSC 19	ISSCC 19	This Work
Abs. Resol. (Meas. Cap)	116aF (40ff)	290aF (N.A)	3.68aF (10ff)
Cap. Range (pF)	0-18.12	0-5	0-18
Power	3μW	6.64μW	71.2μW
FoM _w (fJ/c.step)	660	16	373
FoM _ε (dB)	159.9	156.5	182.8

Comparison Table

2021 IDEC Congress CDC

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.